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Title:

PROGRAMMABLE CONDUCTOR RANDOM ACCESS MEMORY AND METHOD FOR SENSING SAME

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TITLE OF INVENTION

PROGRAMMABLE CONDUCTOR RANDOM ACCESS MEMORY AND METHOD FOR SENSING SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention:

[0001]   The present invention relates to integrated memory circuits. More specifically, it relates to a method for sensing the content of a programmable conductor random access memory (PCRAM) cell.

2. Description of Prior Art:

[0002]   DRAM integrated circuit arrays have existed for more than thirty years and their dramatic increase in storage capacity has been achieved through advances in semiconductor fabrication technology and circuit design technology. The tremendous advances in these two technologies have also achieved higher and higher levels of integration that permit dramatic reductions in memory array size and cost, as well as increased process yield.

[0003]   A DRAM memory cell typically comprises, as basic components, an access transistor (switch) and a capacitor for storing a binary data bit in the form of a charge. Typically, a charge of one polarity is stored on the capacitor to represent a logic HIGH (e.g., binary "1"), and a stored charge of the opposite polarity represents a logic LOW (e.g., binary "0"). The basic drawback of a DRAM is that the charge on the capacitor

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eventually leaks away and therefore provisions must be made to "refresh" the capacitor charge or else the data bit stored by the memory cell is lost.

[0004]   The memory cell of a conventional SRAM, on the other hand, comprises, as basic components, an access transistor or transistors and a memory element in the form of two or more integrated circuit devices interconnected to function as a bistable latch. An example of such a bistable latch is cross-coupled inverters. Bistable latches do not need to be "refreshed," as in the case of DRAM memory cells, and will reliably store a data bit indefinitely as long as they continue to receive supply voltage.

[0005]   Efforts continue to identify other forms of non-volatile or semi-volatile memory elements. Recent studies have focused on resistive materials that can be programmed to exhibit either high or low stable ohmic states. A programmable resistance element of such material could be programmed (set) to a high resistive state to store, for example, a binary "1" data bit or programmed to a low resistive state to store a binary "0" data bit. The stored data bit could then be retrieved by detecting the magnitude of a readout current switched through the resistive memory element by an access device, thus indicating the stable resistance state it had previously been programmed to.

[0006]   Recently programmable conductor memory elements have been devised. For example, chalcogenide glasses which have switchable resistive states have been investigated as data storage memory cells for use in memory devices, such as DRAM memory devices. U.S. Patents 5,761,115, 5,896,312, 5,914,893, and 6,084,796 all describe this technology and are incorporated herein by reference. One characteristic of a programmable conductor memory element such as one formed of the chalcogenide glasses described above is that it typically includes chalcogenide glass which can be doped with metal ions and a cathode and anode spaced apart on one or more surfaces of the glass. The doped glass has a normal and stable high resistance state. Application of a voltage across the cathode and anode causes a stable low resistance path to occur in the glass. Thus, stable low and high resistance states can be used to store binary data.

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[0007]   A programmable conductor memory element formed of a doped chalcogenide glass material typically has a stable high resistance state which may be programmed to a low resistance state by applying a voltage across the memory element. To restore the memory cell to a high resistive state, typically one needs to program the cell with a negative, or inverse voltage which is equal to or greater that the voltage used to program the memory element to the low resistance state. One particularly promising programmable conductor chalcogenide glass has a Ge:Se glass composition and is doped with silver.

[0008]   Suitable circuitry for reading data from an array of programmable conductor memory elements has not yet been fully developed. Accordingly, in order to realize a functional programmable conductor memory, appropriate read circuitry is required to nondestructively sense data stored in the memory elements of the array.

SUMMARY OF THE INVENTION

[0009]   A sense circuit for reading a resistance level of a programmable conductor random access memory (PCRAM) cell is provided. A voltage potential difference is introduced across a PCRAM cell by activating an access transistor from a raised rowline voltage. Both a digit line and a digit complement reference line are precharged to a first predetermined voltage. The cell being sensed has the precharged voltage discharged through the resistance of the programmable conductor memory element of the PCRAM cell. A comparison is made of the voltage read at the digit line and at the reference conductor. If the voltage at the digit line is greater than the reference voltage, the cell is read as a high resistance value (e.g., logic HIGH); however, if the voltage measured at the digit line is lower than that of the reference voltage, the cell is read as a low resistance value (e.g., logic LOW). In an additional aspect of the invention, in order to rewrite a logic "HIGH" into the cell, the rowline associated with the cell being sensed may be raised to a higher voltage after the cell is sensed.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0010]   The foregoing and other advantages and features of the invention will become more apparent from the detailed description of preferred embodiments of the invention given below with reference to the accompanying drawings in which:

[0011]   Fig. 1 depicts two memory arrays each employing a plurality of PCRAM memory cells, in accordance with an exemplary embodiment of the invention;

[0012]   Figs. 2(a) - 2(d) each depict a PCRAM memory cell of Fig. 1;

[0013]   Fig. 3 depicts an N-sense amplifier as used in the Fig. 1 memory array;

[0014]   Fig. 4 depicts a P-sense amplifier as used in the Fig. 1 memory array;

[0015]   Fig. 5 depicts a flowchart describing an operational flow, in accordance with an exemplary embodiment of the invention;

[0016]   Fig. 6 depicts a timing diagram for a reading of high resistance in a sensed memory cell, in accordance with an exemplary embodiment of the invention;

[0017]   Fig. 7 depicts a timing diagram for a reading of low resistance in a sensed memory cell, in accordance with an exemplary embodiment of the invention; and

[0018]   Fig. 8 depicts a block diagram of a processor-based system containing a PCRAM memory, in accordance with an exemplary embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0019]   The present invention will be described as set forth in exemplary embodiments described below in connection with Figs. 1-8. Other embodiments may be realized and other changes may be made to the disclosed embodiments without departing from the spirit or scope of the present invention.

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[0020] In accordance with an exemplary embodiment of the invention, a pair of memory arrays are coupled to a respective plurality of sense amplifiers where each memory array is made up of a plurality of programmable conductor memory cells. In order to read a logical state of a given memory cell, an appropriate voltage difference must be placed across the programmable conductor memory element. The voltage difference must be sufficient to enable a read operation of the programmable conductor memory element, but insufficient to enable the element to be programmed (or written to). Once the appropriate voltage difference exists across the memory element, a digit (bit) line voltage value is discharged through the memory cell and through the programmable conductor memory element. A predetermined period of time after the discharging begins, a comparison is made, via a sense amplifier associated with the given memory cell, between the digit line voltage and a digit complement reference voltage at a reference bit line.

[0021] If after the predetermined time, the digit line voltage is higher than the voltage at the reference line, then a high resistive state is detected and the reference line is grounded. If, however, the digit line voltage is lower than the voltage at the reference line 106, then a low resistive state is detected and the digit line is grounded. The reference voltage is supplied by a digit complement line associated with an adjacent memory array. The two adjacent memory arrays respectively serve as sources for the a reference voltage when the other of the two memory arrays contains a selected memory cell. Fig. 1 provides greater detail of an exemplary embodiment of the invention.

[0022] Fig. 1 depicts a portion of a pair of memory arrays 100, 165, each having a plurality of columns 108, 112, 106, 110 and rows 122, 126, 128, 124, 130, 132. At each intersection of columns and rows there is formed a programmable conductor random access memory (PCRAM) cell such as memory cell 120. Sense amplifier 102 receives inputs from column line 108 and column line 106. Sense amplifier 104 receives inputs from column line 112 and column line 110. Each sense amplifier 102, 104 is configured to compare a voltage at a digit (bit) line (e.g., 108) of a cell 120 being read with a voltage at a reference line (e.g., 106) in order to determine whether the sensed memory cell 120 is

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storing a value of logic HIGH or logic LOW. In the Fig. 1 arrangement, if cell 120 is being read, a voltage at digit line 108 is compared with a reference voltage on complementary digit line 106 by sense amplifier 102.

[0023]   Depending upon which side of the sense amplifier 102 contains the memory cell 120 of interest, the digit line 108 or 106 acts as the digit line D and the digit line 106 on the other side acts as the reference digit line D*. In this example, it is assumed that memory cell 120 is the cell being sensed. The column line 108 associated with memory cell 120 is referred to as the digit (bit) line D. Column line 106 is referred to as the digit complement line D*, or the reference line.

[0024]   Each programmable conductor memory cell 120 consists of an access transistor 114 and a programmable conductor memory element 116. One end of the programmable conductor memory element 116 is coupled to a cell plate 118. The other end of the programmable conductor memory element 116 is coupled to a source/drain terminal of access transistor 114. Another source/drain terminal of access transistor 114 is coupled to digit line 108. A gate of the access transistor 114 is coupled to a rowline 122 associated with the memory cell 120.

[0025]   Further, the D and D* lines are coupled to a pre-charging circuit 175 for precharging the D and D* lines to a predetermined voltage value (e.g., Vdd). The D* line is coupled to one terminal of p-type complementary metal oxide semiconductor (CMOS) transistor 177 and another terminal of transistor 177 is coupled to Vdd. The D line is coupled to one terminal of p-type CMOS transistor 179 and another terminal of transistor 179 is coupled to Vdd. The gates of both transistors 177, 179 are coupled together for receiving a precharge control signal. When the precharge control signal is received, both transistors 177, 179 are turned on and both the digit line D and digit-complement line D* are charged to Vdd. Fig. 1 also shows an equilibrate circuit 176 for equalizing the voltage on the D and D* digit lines. After the D and D* are precharged to Vdd by a precharge signal, the lines are then equilibrated by an equilibrate EQ signal applied to transistor 180.

[0026]   Turning to Fig. 2(a), a simplified schematic diagram of programmable conductor memory cell 120 is depicted. Using the representative cell 120 to describe the invention, digit line D 108 is coupled to Vdd during precharge and also coupled to a first terminal of access transistor 114. Access transistor 114 is depicted as n-type CMOS transistor; however, access transistor 114 may easily be replaced with a p-type CMOS transistor as long as the corresponding polarities of the other components and voltages are modified accordingly. A second terminal of transistor 114 is coupled to a first terminal of programmable conductor memory element 116. As mentioned above, programmable conductor memory element 116 may be made of chalcogenide glass, or any other bistable resistive material that allows for the storage of binary values. The programmable conductor memory element 116 is coupled to cell plate 118 which is also a common conductor for a plurality of programmable conductor memory elements. The cell plate 118 is tied to a voltage terminal for providing a predetermined voltage level (e.g., Vdd/2) to the cell plate 118. A gate of access transistor 114 is tied to rowline 122. When sufficient voltage is applied to rowline 122, access transistor 114 is turned on and conducting and couples the digit line D 108 to the programmable conductor memory element 116.

[0027]   The voltage value applied to rowline 122 dictates what operation is being performed on the programmable conductor memory element 116. For instance, assuming the D line 108 is tied to Vdd (e.g., 2.5V) and the cell plate is tied to ½ Vdd (e.g., 1.25V), in order to activate the access transistor 114, a minimum of 2.05V must be applied to its gate. A voltage of 2.05V at the gate of access transistor 114 is sufficient to turn on transistor 114 since that creates a difference of potential of at least the threshold voltage (Vt), approximately 0.8V, between the gate and the source/drain terminal coupled to the cell plate 118.

[0028]   While 2.05V applied to the gate of access transistor 114 is sufficient to turn it on, it is not sufficient for reading from or writing to the programmable conductor memory cell 120. In accordance with an exemplary embodiment of the invention, approximately 0.2V is required to be across the programmable conductor memory element 116 in order

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to read it. Further, in order to write (e.g., re-program its value) to the programmable conductor memory element 116, a minimum of 0.25V is required to be across it and the polarity of the 0.25V depends on whether a logic HIGH or a logic LOW is being rewritten to the memory element 116.

[0029]   Turning to Fig. 2(b), the voltage levels and their polarities are discussed in greater detail. For a read operation, since approximately 0.2V is required across the programmable conductor memory element 116, a voltage of approximately 2.25V is applied to the rowline 122 coupled to the gate of access transistor 122. The threshold voltage, Vt, is subtracted from 2.25V and point A is approximately 1.45V. The cell plate being at 1.25V leaves a voltage drop of 0.2V across the programmable conductor memory element 116; a voltage sufficient for reading the contents of the element 116, but insufficient for writing to the element 116.

[0030]   Fig. 2(c) depicts exemplary voltage levels and polarities for writing a logic LOW back into the programmable conductor memory element 116. As will be described in greater detail below, when a logic LOW level has been read as being stored by the programmable conductor memory cell 120, the D line 108 is grounded by the sense amplifier 102. Point A is also at approximately ground and, therefore, a voltage drop of approximately -1.25V is across the programmable contact and the logic LOW may be rewritten back into the programmable conductor memory element 116.

[0031]   Fig. 2(d) depicts exemplary voltage levels and polarities for writing a logic HIGH back into the programmable conductor memory element 116. As will be described in greater detail below, when a logic HIGH level has been read as being stored by the programmable conductor memory cell 120, the D line 108 is boosted to approximately Vdd by the sense amplifier 102. Then, the rowline 122 is raised from approximately 2.25V (its voltage level during the read operation) to approximately Vdd, thereby placing a voltage of approximately 1.7V at point A. The 1.7V at point A creates a potential

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difference of approximately 0.45V across the programmable conductor memory element 116 in order to rewrite the logic HIGH level.

[0032]   Referring back to Fig. 1, the sense amplifier 102 includes an N-sense amplifier portion and a P-sense amplifier portion. Fig. 3 depicts the N-sense amplifier portion 350. A first terminal of N-sense amplifier 350 receives digit complement line D* (i.e., the column line in the memory array adjacent to the memory array that contains the memory cell of interest) and is also coupled to a gate of n-type CMOS transistor 305 and a first terminal of n-type CMOS transistor 300. A second terminal of N-sense amplifier 350 receives digit line D (i.e., the column line in the memory array that contains the cell of interest) and is also coupled to a gate of transistor 300 and a first terminal of transistor 305. A second terminal of transistor 300 and a second terminal of transistor 305 are coupled to a first terminal of CMOS transistor 310. A second terminal of transistor 310 is coupled to ground and a gate of transistor 310 receives a Fire N control signal. The Fire N control signal is received by the N-sense amplifier 350 a predetermined time after the desired memory cell rowline is fired, as will be described below.

[0033]   Fig. 4 depicts a P-sense amplifier portion 360 of a sense amplifier such as sense amplifier 102. A first terminal of P-sense amplifier 360 receives digit complement line D* and is also coupled to a gate of p-type CMOS transistor 330 and a first terminal of p-type CMOS transistor 325. A second terminal of P-sense amplifier 360 receives digit line D and is also coupled to a gate of transistor 325 and a first terminal of transistor 330. A second terminal of transistor 325 and a second terminal of transistor 330 are coupled to a first terminal of transistor 320. A gate of transistor 320 receives a Fire P control signal. The Fire P control signal is received by the P-sense amplifier 360 a predetermined time after the Fire N control signal is received by the N-sense amplifier 350.

[0034]   Turning to Fig. 5, a flowchart describing an operational flow of the Figs. 1 and 2 schematic diagrams is depicted, in accordance with an exemplary embodiment of the invention. In this exemplary process flow, the following parameters of the PCRAM cell are

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presumed: i) that the erase voltage to grow a dendrite in programmable conductor memory element 116 switching it to a high resistance state and thus write a logic "1" is 0.25V; (ii) that the erase current is approximately 10µA; (iii) that the program voltage (write a "1" element to logic "0") is –0.25V; (iv) that the program current is approximately 10µA; (v) that the resistance corresponding to a logic "0" is approximately 10KΩ; and (vi) that the resistance corresponding to a logic "1" is any value greater than approximately 10MΩ. It should be readily apparent that alternative parameters and operating voltages and resistances may be selected for the PCRAM cell without departing from the spirit and scope of the invention.

[0035]   The process begins at process segment 500. At segment 502, sense amplifier 102 sees the two lines D and D*, where both D and D* are respective column lines 108, 106 from different memory arrays 100, 165. For purposes of this description, we will assume Vdd is approximately 2.5V. The cell plate 118 is tied to a predetermined voltage (e.g., Vdd/2, or approximately 1.25V) which is either a condition which is present whenever the memory is active, or one which can be switched to by memory operation. In this illustrated embodiment, the Vdd/2 voltage is turned on at processing segment 506. At segment 508, both lines D, D* 108, 106 are precharged to a predetermined voltage (e.g., Vdd = approximately 2.5 V) via precharge circuit 175 and then equilibrated by equilibrate circuit 176.

[0036]   A selected rowline 122 is fired at segment 510 by applying a predetermined voltage from a rowline decoder to that rowline 122. In this example, the predetermined voltage has been selected to be approximately 2.25V as will be described herein. In order to read the contents of the memory cell 120, or more specifically, in order to read the resistance of the programmable conductor memory element 116 of the memory cell 120, a voltage of approximately 0.2V must be present across the element 116. This means that a voltage of approximately 2.25V must be applied to the rowline 122. A voltage of approximately 2.25V applied to rowline 122 turns on transistor 114. Since the threshold voltage of transistor 114 is approximately 0.8V, then a voltage of approximately 1.45V is

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present at point A while a voltage of approximately 1.25V is present at the cell plate 118 for a difference of approximately 0.2V, the required read voltage, as indicated at segment 512 of Fig. 5.

[0037]   It should be mentioned that when access transistor 114 is conducting, the voltage of the digit line D 108 is actually increased by approximately 0.1V (up to approximately 2.6V) due to a parasitic capacitance (e.g., 138 of Fig. 1) inherent between the column line 108 and the rowline 122 of the memory cell. This results in approximately a 0.1V difference between digit line D, the column line 108 associated with the cell being read 120, and D* 106, the reference digit line. The parasitic capacitance 138 may be varied as a function of the construction of the memory cell or an additional capacitance in the form of a fabricated capacitor can also be provided which is switched in circuit and connected with digit line D 108 during a read operation; therefore, in accordance with an exemplary embodiment of the invention, the amount of voltage increase when the rowline 122 is fired can be controlled by the memory architecture. The increase in the voltage at D 108 is described at segment 514.

[0038]   There are other ways to increase the voltage difference between D and D*, as seen by the sense amplifier 102. For instance, a dummy row line 124 could be employed in the memory array that is not of interest (e.g., 165) such that the dummy rowline 124 is always on and precharged to Vdd (approximately 2.5V). Then, when the desired rowline 122 is fired, and the desired digit line D 108 is raised to approximately 2.6V, due to the parasitic capacitance 138, the dummy rowline 124 is turned off and, as a result, the voltage at digit complement line D* 106 drops to approximately 2.4V due to the parasitic capacitance 138 between the dummy rowline 124 and column line 106. The end result is that D 108 and D* 106 differ by at least approximately 0.2V when D 108 begins to discharge as described below.

[0039]   Still referring to Fig. 5, at segment 516, the digit line of interest D 108 begins to discharge from approximately 2.6V through the resistance of the programmable

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conductor memory element down to approximately 1.25V, the cell plate 118 voltage. The longer the discharge operation takes, the greater the resistance level of the programmable conductor memory element 116. A predetermined time (e.g., 15-30ns) after the selected rowline 122 is fired, at segment 510, the N-sense amplifier 350 is enabled, via control signal Fire N, at segment 518 which compares the voltage on the D 108 and D* 106 lines. At segment 520, a determination is made as to whether the programmable conductor element 116 has a low or high resistance level.

[0040] For example, at segment 522, a determination is made as to whether the initial voltage on D 108 has discharged below the voltage on D* 106 in the predetermined timeframe (e.g., 15-30ns). Referring back to Fig. 3, the voltage values at D* 106 and D 108 are respectively fed to gates of transistors 305 and 300. If at the predetermined time t_2, the voltage at the digit line D 108 is higher than the voltage at the digit complement line D* 106, then D* 106 is grounded and D remains floating and considered as having a high resistance level (e.g., logic HIGH) at segment 524.

[0041] It should be noted that rowline 122 may be turned off after the access transistor 114 is turned on. Doing so, however, will present the programmable conductor memory element 116 from being re-written. This may be desired when a logic HIGH was read since a re-write may not be desired after each read operation of a logic HIGH as this is the normal state of the programmable conductor memory element 116 and repeated unnecessary re-writing may result in damage to the element 116 over time.

[0042] Still referring to segment 522, if at the predetermined time t_2, the voltage at D 108 is lower than that at D* 106, then line D 108 is grounded and D 108 is considered as having a low resistance level (e.g., logic LOW) at segment 526.

[0043] At segment 528, P-sense amplifier 360 is enabled, via control signal Fire P, a predetermined time (e.g., 1-5ns) t_3 after the N-sense amplifier 350 is enabled. If a high resistance level was recognized at segment 524 (i.e., D 108 is logic HIGH), then transistor

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330 is on and transistor 325 is off and the voltage at line D 108 is boosted to approximately Vdd at segment 530.

[0044]   If a low resistance level was recognized at segment 524 (i.e., D 108 is logic LOW), then transistor 330 is off and transistor 325 is on and line D* 106 is maintained at approximately Vdd at segment 532.

[0045]   At segment 534, the rowline 122 voltage is raised to approximately Vdd. If the programmable conductor memory element 116 contained a low resistive state, then, as described above, raising the rowline 122 voltage to approximately Vdd is not necessary to re-write a low resistive state; however, the rowline 122 is nonetheless raised in order to facilitate re-writing a high resistance state. That is, if the programmable conductor memory element 116 contained a high resistive state, then raising the rowline 122 to approximately Vdd sets the voltage at point A to approximately 1.7V, thereby placing a voltage potential difference of approximately 0.45V across the programmable conductor memory element 116 which is sufficient for re-writing.

[0046]   Fig. 6 depicts a timing diagram showing a process flow for finding a high resistance level, as described in connection with a portion of Fig. 5. For example, initially, both D 108 and D* 106 are precharged to approximately Vdd. At time t_1, rowline 122 fires and turns on transistor 114. The voltage at D 108 increases by approximately 0.1V to approximately 2.6V due to the parasitic capacitance 138 between rowline 122 and column line 108. Then, line D 108 is discharged from approximately 2.6V for approximately 15-30ns while line D* 106 is maintained at approximately Vdd. At time t_2, N-sense amplifier 350 is enabled and compares the voltage at line D 108 with that of line D* 106. If the voltage measured at D 108 is greater than that of D* 106, then a high resistance level is recognized, as described in connection with Fig. 5. In addition, line D* 106 is forced to ground (0V) at time t_2. At time t_3, P-sense amplifier 360 is enabled and line D is boosted to Vdd and read as logic HIGH. At time t_4, the rowline 122 voltage is increased from

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approximately 2.25 to approximately Vdd, thereby enabling the contents of the programmable conductor element 116 to be rewritten.

[0047] Fig. 7 depicts a timing diagram showing a process flow for finding a low resistance level, as described in connection with a portion of Fig. 5. For example, initially, both line D 108 and line D* 106 are precharged to approximately Vdd. At time t_1, rowline 122 fires and turns on transistor 114. The voltage at D 108 increases by approximately 0.1V to approximately 2.6V due to parasitic capacitance 138. Then, D 108 is discharged from approximately 2.6V for approximately 15-30ns while D* 106 is maintained at approximately Vdd. At time t_2, N-sense amplifier 350 is enabled and compares the voltage at line D 108 with that of line D* 106. If the voltage measured at D 108 is less than that of D* 106, then a low resistance level is recognized, as described in connection with Fig. 5. In addition, line D 108 is forced to ground (0V) at time t_2. At time t_3, P-sense amplifier 360 is enabled and line D remains at 0V and is read as logic LOW and line D* is maintained at approximately Vdd. At time t_4, rowline 122 voltage is increased from approximately 2.25 to approximately Vdd. As described above, although this is not necessary to re-write a low resistance level in the programmable conductor memory element 116, it is done so that other memory cells storing a high resistance level may be re-written.

[0048] Fig. 8 illustrates a block diagram of a processor system 800 containing a PCRAM semiconductor memory as described in connection with Figs. 1-7. For example, the PCRAM memory arrays 100, 165 described in connection with Figs. 1-7 may be part of random access memory (RAM) 808 which may be constructed as a plug-in module containing one or more memory devices having the PCRAM structure described above. The processor-based system 800 may be a computer system or any other processor system. The system 800 includes a central processing unit (CPU) 802, e.g., a microprocessor, that communicates with floppy disk drive 812, CD ROM drive 814, and RAM 808 over a bus 820. It must be noted that the bus 820 may be a series of buses and bridges commonly used in a processor-based system, but for convenience purposes only, the bus 820 has been

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illustrated as a single bus. An input/output (I/O) device (e.g., monitor) 804, 806 may also be connected to the bus 820, but are not required in order to practice the invention. The processor-based system 800 also includes a read-only memory (ROM) 800 which may also be used to store a software program.

[0049]   Although the Fig. 8 block diagram depicts only one CPU 802, the Fig. 8 system could also be configured as a parallel processor machine for performing parallel processing. As known in the art, parallel processor machines can be classified as single instruction/multiple data (SIMD), meaning all processors execute the same instructions at the same time, or multiple instruction/multiple data (MIMD), meaning each processor executes different instructions.

[0050]   The present invention provides a PCRAM cell 120 and a method for reading the contents of the memory cell 120. The memory cell 120 consists of a programmable conductor memory element 116 in series with a first terminal of an access transistor 114. The other side of the programmable conductor memory element 116 is coupled to a cell plate 118 that may extend across a plurality of programmable conductor memory elements 116. A second terminal of the access transistor 114 is coupled to a column line 108, which can be the desired digit line (D). The gate of the transistor 114 is coupled to the rowline 122 of the memory cell 120. A first predetermined voltage potential (e.g., Vdd) is applied to digit line D 108 and a reference digit line D* 106 of an adjacent memory array 165. A second predetermined voltage potential is applied to the cell plate 118. When the rowline 122 for a desired memory cell 120 is fired with a third predetermined voltage potential (e.g., approximately 2.25V), the access transistor 114 is turned on and conducts and digit line D 108 discharges for a predetermined time period (e.g., 15-30ns) at which time, line D 108 and line D* 106 are compared with each other, with sense amplifier 102, in order to determine whether the programmable conductor element 116 contains a high or low resistance level. The memory cell 120 being read is then prepared for a next cycle by precharging both line D 108 and line D* 106, as well as the rowline 122 voltage, up to approximately Vdd so that the high resistance level may be rewritten to the memory cell

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120 if the memory cell did in fact have a high resistance level. If the memory cell 120 had a low resistance level, then raising the voltage potentials of lines D 108 and D* 106 and the rowline 122 will have no effect on the resistance of the memory cell 120.

[0051]   While the invention has been described in detail in connection with preferred embodiments known at the time, it should be readily understood that the invention is not limited to the disclosed embodiments. Rather, the invention can be modified to incorporate any number of variations, alterations, substitutions or equivalent arrangements not heretofore described, but which are commensurate with the spirit and scope of the invention. For example, although the invention has been described in connection with specific voltage levels, it should be readily apparent that voltage levels very different than those described herein can be used to achieve the same results. In addition, although the invention has been described in connection with n-type and p-type CMOS transistors, it should be readily apparent that complementary CMOS transistors can be used instead. Furthermore, although the invention has been described in connection with a specific polarity for the memory cell 120, that polarity may be reversed resulting in different voltage levels being applied to the transistor 114, cell plate 118, digit line D 108 and digit complement line D* 106. Accordingly, the invention is not limited by the foregoing description or drawings, but is only limited by the scope of the appended claims.

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